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A Highly Robust Single-Loop Current Control Scheme for Grid-Connected Inverter with an Improved *LCCL* Filter Configuration

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***Abstract*—Single-loop current control is an attractive scheme for the *LCL*-type grid-connected inverter due to its simplicity and low cost. However, conventional single-loop control schemes, which command either the inverter current or the grid current, are subject to the specific resonance frequency regions. The weighted average current control, which splits the filter capacitor into two parts (in form of an *LCCL* filter) and commands the current flowing between these two parts, is independent of the resonance frequency, but on the other hand, it is limited by the poor sensitivity to the grid impedance variation and weak stability in the grid current. These limitations are comprehensively explained in this paper and then addressed by identifying that the single-loop weighted average current control is equivalent to the dual-loop grid current control with an inherent capacitor current active damping. By tuning the capacitor split proportion as a second degree of freedom, an optimal damping performance that is robust to the grid impedance variation can be naturally achieved using only the inherent damping. Thus, no extra damping is required, and the single-loop structure with only one current sensing turns to be adequate. Moreover, for convenience of practical implementation, an improved *LCCL* filter configuration is proposed to allow the use of two equal nominal capacitances for the split capacitors. Finally, experiments are performed to verify the effectiveness of the proposed method.**

***Index Terms*—Active damping, grid impedance, grid-connected inverter, *LCCL* filter, single-loop control.**

I. Introduction

As an efficient power conversion interface, the grid-connected inverter with an *LCL* filter has been widely used to convert the dc power to the high-quality ac power and feed it into the grid [1]–[4]. The use of *LCL* filter offers an effective attenuation of the switching harmonics, but it faces also potential resonance problems [5]–[8]. Fortunately, without damping the *LCL*-filter resonance, a single-loop control scheme, which commands either the inverter current or the grid current, is found to be possible to stabilize the system. The stability of such a single loop depends on the ratio of the resonance frequency f_r to the sampling frequency f_s, due to the computation and pulse-width modulation (PWM) delays. With a total delay of T_d, the critical resonance frequency f_{crit} is proved to be $1/(4T_d)$ [9], [10]. The stable region is $f_r < f_{\text{crit}}$ for the inverter current control and $f_r > f_{\text{crit}}$ for the grid current control. Typically, $T_d = 1.5T_s$ (T_s is the sampling period), thus $f_{\text{crit}} = f_s/6$ [11]–[13]. To retain a stable operation, the *LCL* filter should be carefully designed with its resonance frequency falling into the stable region [14], [15]. Note that a lower f_r calls for larger filter inductors or filter capacitor, thereby $f_r > f_s/6$ would be most cost-effective. This is, however, not always possible in practice, since the variation of grid impedance may shift f_r across $f_s/6$ [16].

To address this issue, an intuitive method is to widen the stable region, so that it can tolerate a wider range variation of the resonance frequency. Achieving this goal, for the inverter current control, requires to increase f_{crit} by reducing the delay T_d, whereas to decrease f_{crit} by adding another delay to T_d for the grid current control. The additional delay will impose a further limitation on the control bandwidth and thus it is not generally recommended. When it comes to the delay reduction, the state observer [17], the real-time sampling and update schemes [18]–[20], and the phase-lead compensators [21]–[25] can be used. To avoid the model-dependent nature of the state observer, a real-time sampling scheme, which shifts the sampling instant towards the PWM reference update instant, is proposed in [18]. Although it is simple, the implementation is susceptible to aliasing due to the asynchronous sampling process. An alternative solution is to update the PWM reference immediately after it is being computed while keeping the synchronous sampling. In this way, the aliasing is avoided, but the computation time for controller processing must be very short and not exceed $0.25T_s$ [19], [20]. Thus, it is mainly suitable for high-power application where the switching/sampling frequency is relatively low. Phase-lead compensation can be achieved with a lead-lag element [21], a first-order lead compensator [22], [23], and a second-order generalized integrator [24]. A graphical evaluation of these

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methods is presented in [25], which reveals that they can compensate a maximum delay of a half sampling period but also lead to the amplification of high frequency noise. Therefore, it is difficult to perform a practical delay reduction with a little side effect.

Besides controlling the inverter current or the grid current, an interesting single-loop scheme, which controls their weighted average value, is proposed in [26]–[29]. The weighted average current can be obtained by either splitting the capacitor of the *LCL* filter into two parts (in form of an *LCCL* filter) and measuring the current flowing between these two parts [26], or directly measuring both the inverter current and the grid current and then weighting them [27]–[29]. By selecting a proper weight value, the control system can be degraded from a third-order system to a first-order one, like the *L*-filtered grid-connected inverter. Thus, its target control variable, i.e., the weighted average current, is exempt from the *LCL*-filter resonance and can easily be stabilized. However, the reduction of control order relies on an exact knowledge of the grid inductance, which means it is sensitive to the grid impedance variation. Moreover, recent research in [30] shows that even if the control order can be reduced, an implicit resonance hazard still exists in both the inverter current and the grid current, and it will lead to the *critically stable* operations of these two currents. An extra active damping, e.g., the capacitor current active damping [31], can be introduced as an inner loop to solve these problems. Although effective, it looses the benefits of the single-loop control in terms of simplicity and cost.

A robust and practical single-loop current control scheme is therefore urgently demanded. Without any delay addition or reduction, the single-loop weighted average current control is the focus in this paper, and it is implemented by the *LCCL* filter method with only one current sensor being used. The objective of the weighted average current control is to improve the system robustness in our work, rather than to reduce the control order in conventional applications. Through transformation of the control block diagram, the single-loop weighted average current control is found to be equivalent to the dual-loop grid current control with an inherent capacitor current active damping. This inherent damping is determined by the proportion of the split capacitor (i.e., weight value), which if properly designed, can yield an *optimal damping* performance that is robust to the grid impedance variation. Thus, no extra damping is required, and the advantages of the single-loop control are preserved. Upon drawing such method, the practical issue, such as the nominal capacitance, is taken into account. An immediate influence brought by this issue is the deviation of the optimal damping. To compensate for this, an improved *LCCL* filter configuration is proposed.

This paper begins with a discussion on the limitations of conventional weighted average current control in Section II. To break the limitations, a robust single-loop weighted average current control with an optimal inherent damping is proposed in Section III. The proposed method is drawn based on a system with a random time delay, thus it is applicable to different PWM update schemes. The improved *LCCL* filter configuration, which makes the proposed method more practical, is elaborated in Section IV. Experimental results are provided to confirm the theoretical expectations in Section V. Meanwhile, effects of the parasitic resistor and the capacitance deviation are also verified in this section. Finally, Section VI concludes this paper.

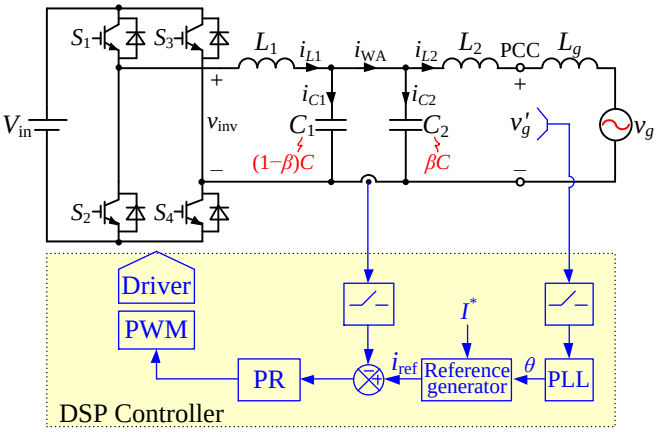

Fig. 1. Weighted average current control for a single-phase grid-connected inverter with an *LCCL* filter.

II. Limitations of Conventional Weighted Average Current Control

A. System Description and Modeling

Fig. 1 shows a single-phase voltage-source inverter feeding into the grid through an *LCL* filter. For convenience of illustration, the *LCL* filter is shown in form of an *LCCL* topology, where the capacitor C is split into two parts C_1 and C_2. L_1 is the inverter- side inductor, L_2 is the grid-side inductor, and L_g is the grid inductance at the point of common coupling (PCC). Depending on the grid configuration, L_g may vary in a wide range, which thus calls for a robust control scheme in order to stabilize the system.

Such a robust operation is usually performed by controlling either the inverter current i_{L1} or the grid current i_{L2} with an extra active damping [30], i.e., a dual-loop strategy. Here, it is evaluated based on a single-loop scheme, which commands the weighted average value of i_{L1} and i_{L2}. Referring to Fig. 1, if the proportions of C_1 and C_2 are $1-\beta$ and β with respect to the total capacitance C, i.e., $C = C_1 + C_2$, $C_1 = (1-\beta)C$, and $C_2 = \beta C$, then $i_{C1} = (1-\beta)i_C$ and $i_{C2} = \beta i_C$, where i_{C1}, i_{C2}, and i_C are the currents of C_1, C_2, and C, respectively. Hence, the current flowing between C_1 and C_2 can be obtained as

$$i_{\mathrm{WA}} = i_{L2} + i_{C2} = i_{L2} + \beta i_C = i_{L2} + \beta\left(i_{L1} - i_{L2}\right) = \beta i_{L1} + \left(1-\beta\right) i_{L2}. \quad (1)$$

Eq. (1) indicates that i_{WA} is exactly the target weighted average current, with β and $1-\beta$ being the weight values of i_{L1} and i_{L2}. Thus, by adopting the *LCCL* topology, i_{WA} can be directly measured with only one current sensor, which surely saves the cost.

A phase-locked loop (PLL) is used to synchronize the inverter with the PCC voltage v_g'. The phase angle extracted by the PLL and the demanded current amplitude I^* are sent to a reference generator to generate the current reference i_{ref}. The

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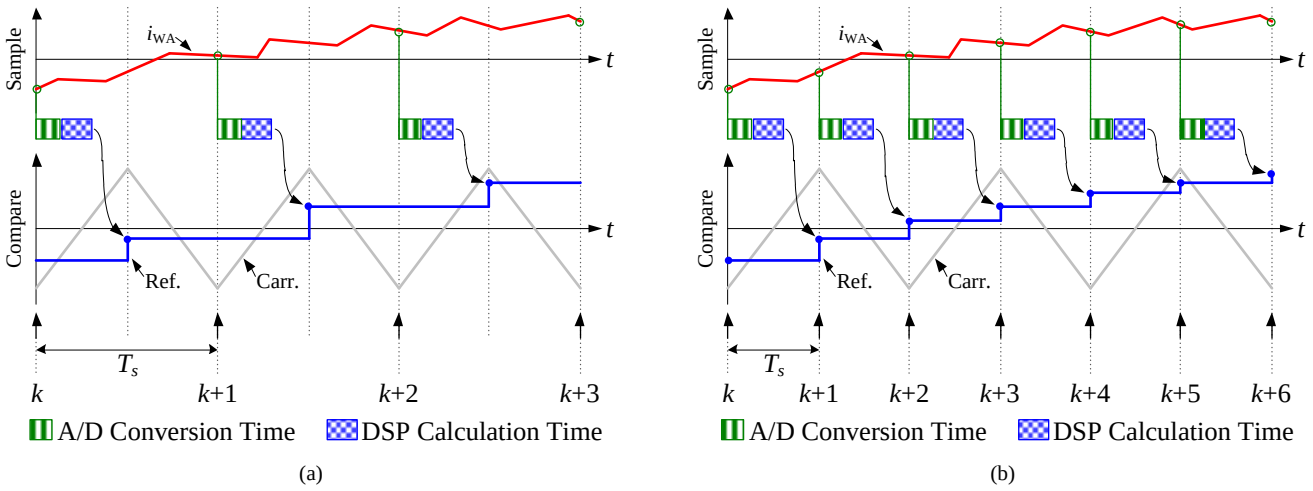

Fig. 2. Computation and PWM delays inherent in the digital PWM. (a) Single update mode, $T_d = T_s$ ($f_s = f_{sw}$). (b) Dual update mode, $T_d = 1.5T_s$ ($f_s = 2f_{sw}$).

phase shift caused by L_2–C_2 is compensated in this generator in order to control the power factor on the grid side. i_{WA} is compared to i_{ref}, and the error signal is sent to a proportional-resonant (PR) regulator, whose output is then fed to a digital PWM modulator.

The digital modulator contains computation and PWM delays [10], [32], [33]. The delay mechanism is shown in Fig. 2, where two PWM update modes are considered. In the single update mode, the sampling is taken either at the beginning or in the middle of a switching period, which means the sampling frequency f_s is equal to the switching frequency f_{sw}. Provided that the total time for A/D conversion and DSP calculation is shorter than $0.5T_s$, the modulation reference can be updated just until the middle of the sampling period (rather than the end), giving a computation delay of $0.5T_s$. In the dual update mode, samplings are taken both at the beginning and in the middle of a switching period, i.e., $f_s = 2f_{sw}$ (twice that in the single update mode), and the modulation reference is updated at the end of the sampling period, giving a computation delay of T_s. For convenience of illustration, the computation delay is defined as λT_s ($0.5 \le \lambda \le 1$), and it is expressed as $e^{-s\lambda T_s}$.

The PWM delay is caused by the zero-order hold (ZOH) effect which keeps the modulation reference constant after it has been updated, and it is definitely $0.5T_s$ in either mode. Thereby, the dual update mode which has a smaller T_s, and thus a smaller delay, is more attractive in practice. For the sake of generality, both modes are analyzed here, and the total delay is $T_d = (\lambda+0.5)T_s$.

A block diagram that accounts for these delays is shown in Fig. 3, where i_{WA} is depicted by the summation of i_{L2} and βi_C referring to (1). $G_i(z)$ is the PR regulator. $G_h(s)$ is the transfer function of the ZOH, and it is expressed as

$$G_h(s) = \frac{1-e^{-sT_s}}{s}. \tag{2}$$

$K_{PWM} = V_{in}/V_{tri}$ is the gain of the PWM inverter, where V_{in} is the input voltage, and V_{tri} is the amplitude of the triangular carrier. $G_{iC}(s)$ and $G_{iL2}(s)$ are the transfer functions from the inverter output voltage $v_{inv}(s)$ to $i_C(s)$ and $i_{L2}(s)$, and they are expressed as

$$\begin{aligned} G_{iC}(s) &= \frac{i_C(s)}{v_{inv}(s)} = \frac{1}{L_1}\cdot\frac{s}{s^2+\omega_r^2} \\ G_{iL2}(s) &= \frac{i_{L2}(s)}{v_{inv}(s)} = \frac{1}{s(L_1+L_2+L_g)}\cdot\frac{\omega_r^2}{s^2+\omega_r^2} \end{aligned} \tag{3}$$

where ω_r is the *LCL*-filter resonance angular frequency and expressed as

$$\omega_r = 2\pi f_r = \sqrt{\frac{L_1+L_2+L_g}{L_1(L_2+L_g)C}}. \tag{4}$$

According to (3), the transfer function from $v_{inv}(s)$ to $i_{WA}(s)$, shown as the shaded area in Fig. 3, can be obtained as

$$G_{iWA}(s) = G_{iL2}(s) + \beta G_{iC}(s) = \frac{\beta(L_1+L_2+L_g)s^2+\omega_r^2 L_1}{sL_1(L_1+L_2+L_g)(s^2+\omega_r^2)}. \tag{5}$$

From (5), it can be found that if β is equal to

$$\beta = \frac{L_1}{L_1+L_2+L_g} \tag{6}$$

then the resonant poles and zeros will cancel out with each other, and $G_{iWA}(s)$ can be simplified as

$$G_{iWA}(s) = \frac{1}{s(L_1+L_2+L_g)}. \tag{7}$$

From (7), it is obvious that $G_{iWA}(s)$ is the same as the transfer function of the L filter with $L = L_1 + L_2 + L_g$. That means, by splitting the capacitor with a proportion $\beta = L_1/(L_1+L_2+L_g)$, the control system is degraded from a third-order system to a first-order one, like the L-filtered grid-connected inverter, thus its target control variable i_{WA} can easily be stabilized. This property is identified as the main benefit of the weighted average current control in conventional applications [26]–[29].

To exploit such benefit, the grid inductance L_g should be known exactly to meet the desired split proportion shown in (6). This is difficult for the weak grid conditions, where the varying L_g will lead to the failures in meeting (6) and then the counteraction of the resonance in $G_{iWA}(s)$. As a result, the control performance and system stability will be impaired,

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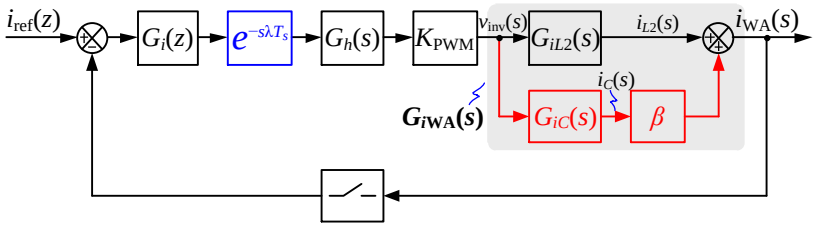

Fig. 3. Block diagram of the weighted average current control.

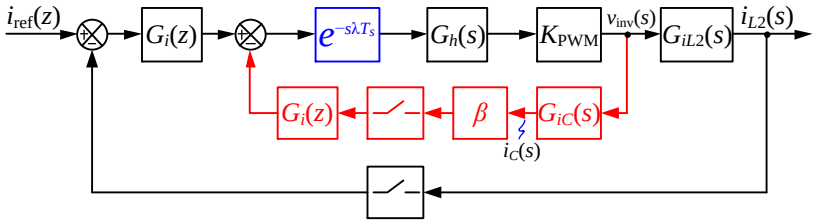

Fig. 4. Equivalent transformation of the block diagram of the weighted average current control.

implying a poor robustness. However, even in a stiff grid where (6) can be perfectly met, there is still a serious stability challenge faced by the grid current. In [30], this stability issue is discussed for $\lambda = 1$. To complete the work, the situation of a random λ is further analyzed as follows.

B. Stability Analysis From the Perspective of Grid Current

Note that the grid current is indirectly controlled and its stability is covered up in the model depicted in Fig. 3. An equivalent transformation of Fig. 3 is made in order to account for the grid current stability. By separating the feedback paths of i_{L2} and i_C, and relocating the feedback node of i_C to the output of $G_i(z)$, an equivalent block diagram is obtained, as shown in Fig. 4. It can be seen that the equivalent model is exactly a dual-loop structure, which involves an outer loop in charge of the grid current control and an inner loop implementing the capacitor current active damping. Moreover, the damping function is $\beta G_i(z)$. This part of damping is not extra introduced, but naturally comes along with the feedback of i_{WA} which contains a part of the capacitor current βi_C [see $i_{WA} = i_{L2} + \beta i_C$ in (1)], thus it is called the inherent damping.

Since i_{L2} is the equivalent target control variable in Fig. 4, its stability now turns to be explicit. To perform an accurate stability analysis in the z-domain, the continuous transfer functions in Fig. 4 are discretized by applying the ZOH transform, as given in (8a) and (8b), where (8b) is shown at the bottom of this page.

$$Z_{\mathrm{ZOH}}\left[G_{iC}(s)e^{-s\lambda T_s}\right]=\frac{z-1}{\omega_r L_1}\cdot\frac{z\sin(1-\lambda)\omega_r T_s+\sin\lambda\omega_r T_s}{z\left(z^2-2z\cos\omega_r T_s+1\right)}. \tag{8a}$$

Then, the system discrete loop gain with regard to i_{L2} can be derived as (9), shown at the bottom of this page.

An interesting feature observed from $T_{iL2}(z)$ is that at the resonance frequency, there is

$$z=z_{1,2}=e^{\pm j\omega_r T_s}\ \Rightarrow\ z^2-2z\cos\omega_r T_s+1=0 \tag{10}$$

and then $T_{iL2}(z)$ can be simplified as

$$\begin{aligned}T_{iL2}\left(z_{1,2}\right)&=-\frac{1}{\beta K_{\mathrm{PWM}}G_i(z)}\cdot\frac{L_1 K_{\mathrm{PWM}}G_i(z)}{L_1+L_2+L_g}\\&=-\frac{1}{\beta}\cdot\frac{L_1}{L_1+L_2+L_g}\end{aligned}. \tag{11}$$

Obviously, for $\beta = L_1/(L_1+L_2+L_g)$, $T_{iL2}(z_{1,2}) = -1$. That means, $z_{1,2}$ is a pair of imaginary roots of the characteristic equation $1+T_{iL2}(z) = 0$, which, in other words, is a pair of closed-loop resonant poles located at the unit circle ($|z_{1,2}| = 1$). Due to this pair of resonant poles, i_{L2} can only be critically stable even though i_{WA} has been stabilized. Moreover, this critically stable feature is deduced based on a random λ, which means it is independent of the time delay. From this point of view, the conventional weighted average current control does not essentially remove the *LCL*-filter resonance, but "hide" it in the grid current.

III. Robust Single-Loop Weighted Average Current Control With Optimal Inherent Damping

As discussed above, the conventional single-loop weighted average current control is limited by its poor robustness and weak stability. To overcome these limitations, an extra active damping, e.g., the capacitor current active damping [31], can be introduced to form a dual-loop strategy. From the

$$Z_{\mathrm{ZOH}}\left[G_{iL2}(s)e^{-s\lambda T_s}\right]=\frac{\omega_r T_s\left[\lambda+(1-\lambda)z\right]\left(z^2-2z\cos\omega_r T_s+1\right)-(z-1)^2\left[z\sin(1-\lambda)\omega_r T_s+\sin\lambda\omega_r T_s\right]}{\omega_r\left(L_1+L_2+L_g\right)z(z-1)\left(z^2-2z\cos\omega_r T_s+1\right)}. \tag{8b}$$

$$\begin{aligned}T_{iL2}(z)&=\frac{K_{\mathrm{PWM}}G_i(z)Z_{\mathrm{ZOH}}\left[G_{iL2}(s)e^{-s\lambda T_s}\right]}{1+\beta K_{\mathrm{PWM}}G_i(z)Z_{\mathrm{ZOH}}\left[G_{iC}(s)e^{-s\lambda T_s}\right]}\\&=\frac{L_1K_{\mathrm{PWM}}G_i(z)}{L_1+L_2+L_g}\cdot\frac{\omega_r T_s\left[\lambda+(1-\lambda)z\right]\left(z^2-2z\cos\omega_r T_s+1\right)-(z-1)^2\left[z\sin(1-\lambda)\omega_r T_s+\sin\lambda\omega_r T_s\right]}{\omega_r L_1 z(z-1)\left(z^2-2z\cos\omega_r T_s+1\right)+\beta K_{\mathrm{PWM}}G_i(z)(z-1)^2\left[z\sin(1-\lambda)\omega_r T_s+\sin\lambda\omega_r T_s\right]}\end{aligned}. \tag{9}$$

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perspective of grid current, the extra damping introduces a second degree of freedom, so that the damping function is not fixed at $\beta G_i(z)$ [where $\beta = L_1/(L_1+L_2+L_g)$ for the control order reduction and $G_i(z)$ is specified by the outer current loop], but it can be tuned to avoid instability. Nevertheless, as a dual-loop control structure, increased cost and control complexity will be results from the extra damping, which are undesirable effects in practice.

In this section, the limitations of conventional weighted average current control are broken without changing its control architecture, i.e., remaining the single-loop manner. Since the reduction of control order doesn't show real advantage, instead, it brings an implicit resonance hazard, there is no need to fix β at $L_1/(L_1+L_2+L_g)$. The split proportion β itself can be tuned as a second degree of freedom to achieve an optimal inherent damping that is robust to a large grid impedance variation.

Recalling Fig. 4, the PR regulator $G_i(z)$ is incorporated in both the outer current loop and the inner active damping loop. For the stability analysis, $G_i(z)$ can be reduced to a proportional gain K_p, since the resonant gain has negligible effect above the fundamental frequency [11]. Thus, the damping function $\beta G_i(z)$ is simplified as a damping gain βK_p, with β being adjustable. Design of this damping gain is constrained by the gain margin (GM) on the loop gain $T_{iL2}(z)$. These constraints have been derived for $\lambda = 1$ in [34], and they are extended to the situation of a random λ in the following section.

In the case of $\lambda = 1$, the gain margins at f_r and $f_s/6$ needs to be concerned to ensure system stability [18], [34]. For a random λ, similar requirements also exist, except that $f_s/6$ is replaced by a general critical resonance frequency f_{crit}, i.e.,

$$f_{\text{crit}} = \frac{1}{4T_d} = \frac{f_s}{4(\lambda+0.5)}. \tag{12}$$

From (12), it is obvious that for $\lambda = 0.5$, $f_{\text{crit}} = f_s/4$; and for $\lambda = 1$, $f_{\text{crit}} = f_s/6$. Substituting $G_i(z) = K_p$ into (9), the gain margins at f_r and f_{crit}, which are denoted by GM_1 and GM_2 (in decibels), respectively, can be obtained as (13a) and (13b), where (13b) is shown at the bottom of this page.

$$\text{GM}_1 = -20\lg\left|T_{iL2}\left(e^{j2\pi f_r T_s}\right)\right| = 20\lg\left(\beta\cdot\frac{L_1+L_2+L_g}{L_1}\right). \tag{13a}$$

In (13b), $K_{\text{d\_crit}}$ is the critical damping gain [18], and it is expressed as

$$K_{\text{d\_crit}} = \begin{cases} \dfrac{\omega_r L_1\cos\omega_r T_s}{K_{\text{PWM}}\sin 0.5\omega_r T_s} & \lambda = 0.5 \\ \dfrac{\omega_r L_1(2\cos\omega_r T_s - 1)}{K_{\text{PWM}}\sin\omega_r T_s} & \lambda = 1 \end{cases}. \tag{14}$$

Similar to the case of $\lambda = 1$, the constraints on GM_1 and GM_2 for a random λ can also be derived, as shown in Table I,

TABLE I
GAIN MARGIN CONSTRAINTS IN THE CONTROL

	Case I	Case II	Case III
Resonance frequency	$f_r < f_{\text{crit}}$	$f_r < f_{\text{crit}}$	$f_r \geq f_{\text{crit}}$
Damping gain	$\beta K_p \leq K_{\text{d\_crit}}$	$\beta K_p > K_{\text{d\_crit}}$	$\beta K_p > 0$
Gain margin constraints	$\text{GM}_1 > 0$ dB	$\text{GM}_1 > 0$ dB, $\text{GM}_2 < 0$ dB.	$\text{GM}_1 < 0$ dB, $\text{GM}_2 > 0$ dB.

where three cases, namely Case I, Case II, and Case III, are defined depending on the resonance frequency and the damping gain.

From (13a), it is found that GM_1 is dependent only on β and filter/grid inductance, and it is equal to 0 dB for $\beta = L_1/(L_1+L_2+L_g)$, which confirms that i_{L2} is critically stable in conventional applications. To improve stability, a modified β can be calculated from (13a) and (13b) to meet the constraints on GM_1 and GM_2. However, as these constraints vary with f_r, selecting β for a specific f_r is not enough, its robustness against the variation of f_r, which is usually caused by the variation of L_g, must be taken into account.

According to (13a) and (13b), the curves of GM_1 and GM_2 with the increase of L_g are depicted in Fig. 5. Although the expressions of GM_2 vary with λ, their trends versus L_g are similar and thus can be represented by one curve. To cover all the three cases listed in Table I, $f_r > f_{\text{crit}}$ is chosen for $L_g = 0$, and it is also an usual situation in practice [6]–[8]. With the increase of L_g, the system moves from Case III into Case II and Case I successively, meanwhile, GM_1 increases and GM_2 decreases. The curves of GM_1 and GM_2 intersects at $f_r = f_{\text{crit}}$, which corresponds to a critical grid inductance L_{g_crit}. Letting $f_r = f_{\text{crit}}$ in (4), L_{g_crit} can be derived as

$$L_{g\_\text{crit}} = \frac{L_1+L_2-L_1L_2C(2\pi f_{\text{crit}})^2}{L_1C(2\pi f_{\text{crit}})^2 - 1}. \tag{15}$$

Note that the gain margin constraints in Case III are exactly in contrary to those in Cases II, and these two cases are bounded by $f_r = f_{\text{crit}}$. If β is designed so that $\text{GM}_1 = \text{GM}_2 = 0$ dB for $f_r = f_{\text{crit}}$ ($L_g = L_{g\_\text{crit}}$), the constraints on GM_1 and GM_2 will be satisfied for all the three cases, as shown in Fig. 5(a). Thus, the system will be stable irrespective of L_g. Substituting $L_g = L_{g\_\text{crit}}$ into (13a), the value of β yielding $\text{GM}_1 = 0$ dB, which is denoted by β_{opt}, can be derived as

$$\beta_{\text{opt}} = \frac{L_1}{L_1+L_2+L_{g\_\text{crit}}}. \tag{16}$$

According to (15) and (16), β_{opt} can be solely determined once the *LCL* filter parameters have been specified. Compared with the conventional $\beta = L_1/(L_1+L_2+L_g)$ in (6), β_{opt} replaces the uncertain L_g with the defined L_{g_crit}. The change seems

$$\text{GM}_2 = -20\lg\left|T_{iL2}\left(e^{j2\pi f_{\text{crit}}T_s}\right)\right| = \begin{cases} 20\lg\left|\dfrac{L_1+L_2+L_g}{K_pL_1}\cdot\dfrac{(K_{\text{d\_crit}}-\beta K_p)\sin 0.5\omega_r T_s}{\sin 0.5\omega_r T_s - 0.5\omega_r T_s\cos\omega_r T_s}\right| & \lambda = 0.5 \\ 20\lg\left|\dfrac{L_1+L_2+L_g}{K_pL_1}\cdot\dfrac{(K_{\text{d\_crit}}-\beta K_p)\sin\omega_r T_s}{\sin\omega_r T_s - \omega_r T_s(2\cos\omega_r T_s - 1)}\right| & \lambda = 1 \end{cases} \tag{13b}$$

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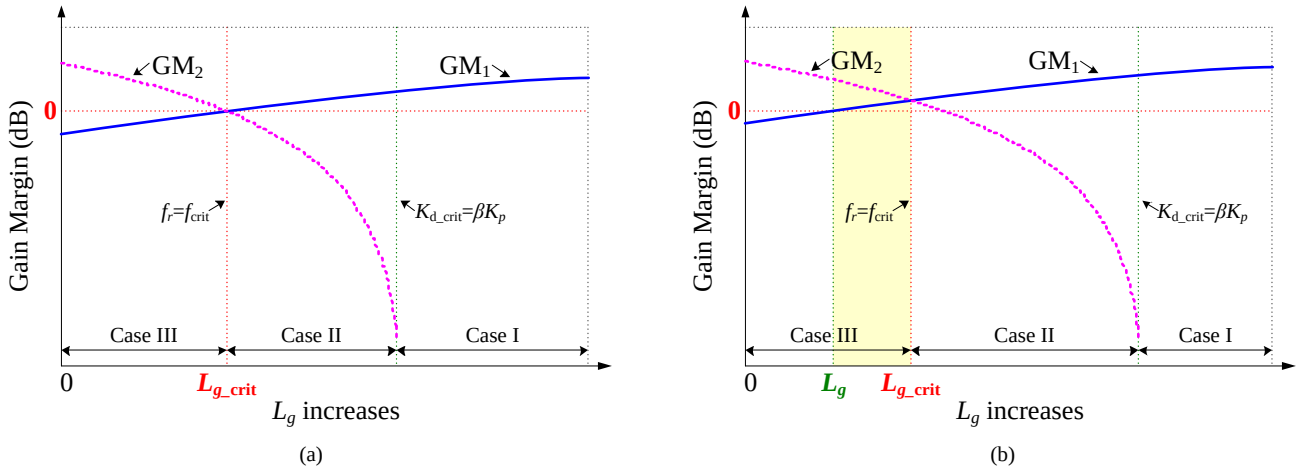

Fig. 5. Curves of GM_1 and GM_2 with the increase of L_g. (a) $\beta = L_1/(L_1+L_2+L_{g\_crit})$. (b) $\beta = L_1/(L_1+L_2+L_g)$.

minor, but its improvement on the system robustness is significant. For example, if $\beta = L_1/(L_1+L_2+L_g)$ is set for an initial L_g that is smaller L_{g_crit}, which implies $\beta > \beta_{opt}$, then with the increase of grid inductance, GM_1 gets larger than 0 dB, as shown in Fig. 5(b). This goes against the gain margin constraints at least in the range between the initial L_g and L_{g_crit} (where $GM_1 < 0$ dB is required), shown as the shaded area in Fig. 5(b), thus leading to instability. Similar instability will arise in the case of $\beta < \beta_{opt}$, which thus comes to the conclusion that β_{opt} is the optimal split proportion.

Aside from the improvement, a special point needs to be concerned that at the particular $f_r = f_{crit}$ ($L_g = L_{g\_crit}$), the system is critically stable due to $GM_1 = GM_2 = 0$ dB. In [34], the stability challenge is addressed by introducing a phase-lag compensator into the current regulator $G_i(z)$. This solution is proposed for the grid current control, unfortunately, it is found useless for the weighted average current control here. In the grid current control, the capacitor current active damping is extra introduced, and its damping performance is independent of $G_i(z)$. Thus, by modifying $G_i(z)$, the loop gain can be adjusted explicitly to ensure stability. However, in the weighted average current control, the capacitor current active damping is inherently existent, and its damping performance is related to $G_i(z)$. That means the outer current loop and the inner damping loop are interacted. Thus, it becomes inexplicit to adjust the loop gain by modifying $G_i(z)$. Recalling (9) and Fig. 4, it is observed that $G_i(z)$ exists in both the numerator and the denominator of $T_{iL2}(z)$, where the former refers to the one located in the outer current loop and the latter refers to the one located in the inner damping loop. Particularly, at the resonance frequency f_r, i.e., $z = z_{1,2}$ [see (10)], the two $G_i(z)$ are cancelled out in $T_{iL2}(z_{1,2})$, as shown in (11), which means $T_{iL2}(z_{1,2})$ is independent of $G_i(z)$. Therefore, even if a phase-lag compensator is added to $G_i(z)$, $T_{iL2}(z_{1,2})$ will remain unchanged and yield $T_{iL2}(z_{1,2}) = -1$ for $L_g = L_{g\_crit}$, implying a critically stable feature. In practice, this small imperfection at such a single point will not cause visible hazard. Moreover, it can be offset by the damping effect of the parasitic resistors in the filter and the grid, which will be discussed later in the next sections.

Another issue should be noted that, although the robust weighted average current control is proposed based on the equivalent dual-loop model, its implementation is still in the single-loop manner with the *LCCL* filter method shown in Fig. 1, except that β is replaced by β_{opt}. Thus, it remains the benefits of the conventional single-loop control.

IV. Improved *LCCL* Filter Configuration Considering the Nominal Capacitance

For implementation of the proposed robust weighted average current control, the capacitor of the *LCL* filter needs to be split with the proportion in (16), i.e., $C_1 = (1-\beta_{opt})C$ and $C_2 = \beta_{opt}C$. Although simple, the calculated values of C_1 and C_2 may not be nominal capacitances. As a result, the actually used capacitances, which must be nominal values, may not match with the calculated (desired) values. This mismatch will cause the actual split proportion deviated from the desired β_{opt}, leading to less robustness. To overcome this drawback, multiple nominal capacitances can be connected in series or in parallel to yield an actual capacitance that equals to the desired one. However, using multiple capacitances for a single filter is not convenient and cost-effective in practice. A practical application would expect to configure two capacitors of the same value, i.e., $C_1 = C_2$, which implies $\beta_{opt} = 0.5$.

Letting $\beta_{opt} = 0.5$ in (16) yields that $L_1 = L_2+L_{g\_crit}$, which upon substituted with (15), gives rise to

$$\frac{1}{2\pi\sqrt{L_1 C}} = \frac{f_{crit}}{\sqrt{2}} \Rightarrow L_1 = \frac{2}{(2\pi f_{crit})^2 C}. \quad (17)$$

According to (17), the requirement on β_{opt} is transferred to the requirement on the resonance frequency between L_1 and C. This can be regarded as an extra constraint on the design of the *LCCL* filter. Besides, there are other well-known constraints, i.e., the inverter-side current ripple is within 15% ~ 40% (peak-to-peak) of the rated current, the capacitive reactive power is less than 5% of the rated load, and the grid-side switching harmonic is less than 0.3% of the rated current [35]–[38]. For the single-phase inverter employing the unipolar sinusoidal PWM, the constraint on the inverter-side current ripple Δi_{L1} is expressed as

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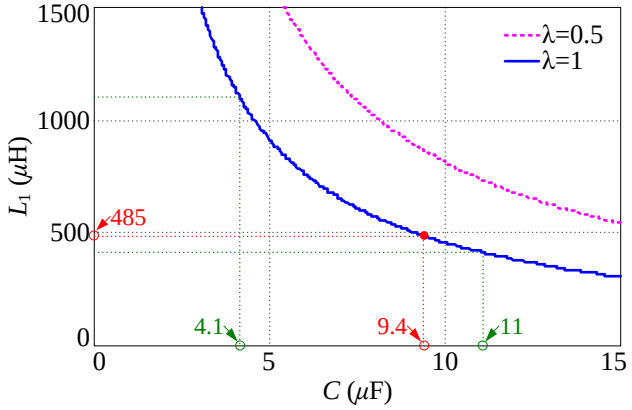

Fig. 6. Curve of L_1 as function of C.

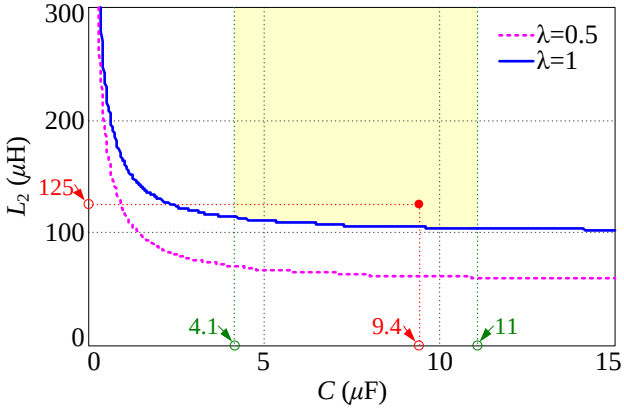

Fig. 7. Curve of L_2 as function of C.

$$15\% \le \frac{\Delta i_{L1}}{I_o} = \frac{V_{\text{in}}}{8L_1 f_{\text{sw}} I_o} \le 40\% \tag{18}$$

where f_{sw} is the switching frequency, and $I_o = P_o/V_g$ is the rated output current, with P_o and V_g being the output power and the grid voltage (RMS), respectively. From (18), the lower and upper limits on L_1 can be obtained, and they are further transferred to the limits on C by substituting (17) into (18) and manipulating, i.e.,

$$\frac{15\% \cdot 16 f_{\text{sw}} I_o}{\left(2\pi f_{\text{crit}}\right)^2 V_{\text{in}}} \le C \le \frac{40\% \cdot 16 f_{\text{sw}} I_o}{\left(2\pi f_{\text{crit}}\right)^2 V_{\text{in}}}. \tag{19}$$

Except for (19), C is also limited by the reactive power drawn from the grid, i.e.,

$$C \le \frac{5\% P_o}{\omega_o V_g^2} \tag{20}$$

where $\omega_o = 2\pi f_o$ is the fundamental angular frequency.

According to (3), the grid-side switching harmonics are expressed as $|I_{L2}(j\omega_h)| = |G_{iL2}(j\omega_h)| \cdot |V_{\text{inv}}(j\omega_h)|$, where ω_h is the harmonic angular frequency and h is the harmonic order. Usually, the dominant harmonic with $\omega_h = 2\pi(2f_{\text{sw}} - f_o)$ is considered, whose harmonic voltage (RMS) is $|V_{\text{inv}}(j\omega_h)| = 20\% V_{\text{in}}$ referring to [39]. Recalling $G_{iL2}(s)$ in (3) and assuming $L_g = 0$ (the worst case for harmonic attenuation), the required L_2 for meeting $|I_{L2}(j\omega_h)| \le 0.3\% I_o$ is obtained as

$$L_2 \ge \frac{1}{\omega_h^2 L_1 C - 1}\left(L_1 + \frac{20\% V_{\text{in}}}{\omega_h 0.3\% I_o}\right). \tag{21}$$

Substituting (17) into (21) yields

$$L_2 \ge \frac{\left(2\pi f_{\text{crit}}\right)^2}{2\omega_h^2 - \left(2\pi f_{\text{crit}}\right)^2}\left(\frac{2}{\left(2\pi f_{\text{crit}}\right)^2 C} + \frac{20\% V_{\text{in}}}{\omega_h 0.3\% I_o}\right). \tag{22}$$

According to (17), (22), and the system parameters listed in Table II, the curves of L_1 and L_2 as function of C are depicted in Fig. 6 and Fig. 7, respectively. Two typical λ, i.e., λ = 0.5 and λ = 1, are both considered here. In order to meet the constraint in (17), the selected L_1 and C must be a point located exactly on the curve in Fig. 6. While in Fig. 7, the satisfactory L_2 and C is the region above the curve, shown as the shaded area (taking λ = 1 for example), whose lower limit is defined by (22). Therefore, selection of L_2 is much more flexible, but it is recommended to be close to the lower limit for the cost-effective purpose.

Taking the system parameters listed in Table II and λ = 1 as an instance, a three-step design procedure of the *LCCL* filter is presented as follows. As the capacitor is the component of most concern, it is designed at first.

1) Determine the possible range of the capacitor, select a proper one and then split it. 4.1 μF ≤ C ≤ 11 μF and C ≤ 20 μF are obtained from (19) and (20), respectively. Thus, the former is taken as the possible range. As shown in (17) and Fig. 6, L_1 is inversely proportional to C. A relatively large C is suggested to lower L_1, and it should be twice the nominal capacitance for convenience of splitting. Here, C = 9.4 μF is selected and split into $C_1 = C_2$ = 4.7 μF, with a total reactive power of 2.4%.
2) Calculate L_1 according to (17). Substituting C = 9.4 μF into (17) yields L_1 = 485 μH, whose location is identified in Fig. 6. Recalling (18), the consequent inverter-side current ripple can be calculated as 34%.
3) Select a proper L_2 from the satisfactory region in Fig. 7. With C = 9.4 μF, the lower limit of L_2 is obtained as L_2 ≥ 105 μH from (22). Here, L_2 = 125 μH is selected with some margin being reserved, as shown in Fig. 7.

It is worth noting that the above design procedure is a step-by-step approach without any trial and error. Based on the selected filter parameters, the initial *LCL* resonance frequency under $L_g = 0$ is calculated as f_r = 5.2 kHz from (4), and the critical grid inductance obtained from (15) is L_{g_crit} = 360 μH, which certainly meets $L_1 = L_2 + L_{g\_\text{crit}}$ as expected.

For λ = 0.5, the same design procedure can be applied, and it is not repeated. The design results are given as L_1 = 495 μH, $C_1 = C_2$ = 8.2 μF, and L_2 = 80 μH. Thus, the initial resonance frequency is 4.8 kHz, which is comparable to that in λ = 1.

V. Experimental Verification

A. Prototype Description

To verify the theoretical analysis, a 6-kW prototype of Fig. 1 was built and tested in the lab. Its photograph is given in Fig. 8. The single-phase inverter bridge was implemented using two IGBT modules (CM100DY-24NF). These modules were driven by M57962L. The PCC voltage v_g', which was used in the PLL, was sensed by a voltage hall (LV25-P). The weighted average current i_{WA} was sensed by a current hall (LA55-P). The measured signals were filtered by a RC low-pass filter

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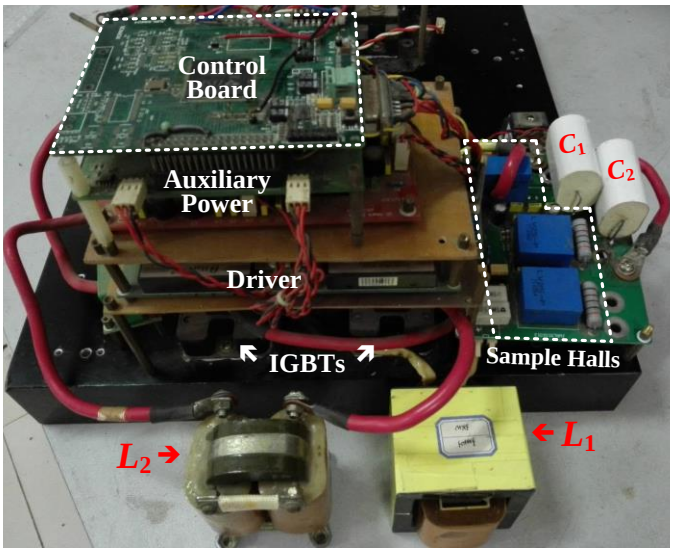

Fig. 8. Photograph of the single-phase grid-connected inverter prototype.

with the time constant of 1 μs, before they were sent to an extended 14-bit A/D converter (MAXIM-1324ECM). Finally, the outputs of the A/D converter were transmitted to a TI TMS320F2812 DSP for the controller process.

The system parameters, together with the *LCCL* filter parameters designed in Section IV, are given in Table II. The unipolar sinusoidal, dual-update PWM was mainly implemented due to its smaller time delay, and $f_s = 2f_{sw} = 20$ kHz was set. The inverter-side inductor L_1 conducted abundant high-frequency ripple current, and it was fabricated by two pairs of EE70/33/32 ferrite cores to lower the loss. The grid-side inductor L_2 conducted only the fundamental current, and it was fabricated by the silicon-steel core to reduce the cost. Film capacitors produced by EACO STH series [40] were adopted as the filter capacitors C_1 and C_2. The current controller is designed for these system settings, and the system stability is examined against the varying grid inductance. Typically, L_g varying up to 10% per unit, which corresponds to 2.6 mH in the test system, is considered.

For the PR regulator adopted, its continuous transfer function is expressed as

$$G_i(s) = K_p + \frac{2K_r\omega_i s}{s^2 + 2\omega_i s + \omega_o^2} \tag{23}$$

where ω_i is the resonant cut-off frequency. In view of a typical ±1% variation of the fundamental frequency [16], ω_i = 1%·2πf_o = π rad/s is set. The proportional gain K_p is designed to achieve a target crossover frequency f_c with a phase margin of 45°, and the resonant gain K_r is tuned with its corner frequency being a decade below f_c [32]. In this way, K_p = 0.07 and K_r = 10 are chosen. For practical use, the PR regulator is decomposed into two simple integrators, where the direct integrator is discretized by forward Euler and the feedback one is discretized by backward Euler [41]. Thus, the discrete representation of $G_i(s)$ is obtained as

$$G_i(z) = K_p + \frac{2K_r\omega_i T_s (z-1)}{z^2 + z\left(\omega_o^2 T_s^2 + 2\omega_i T_s - 2\right) - 2\omega_i T_s + 1}. \tag{24}$$

As discussed in previous sections, the split proportion β is the most important term that affects the system stability. To provide a comparative study, two β drawn in different design procedures are evaluated. One is the proposed $\beta_{opt} = L_1/(L_1+L_2+L_{g\_crit})$, and it is specified to β_{opt} = 0.5 with the improved filter configuration in Section IV, whose corresponding *LCCL* filter is identified as Filter I in Table II. The other is the conventional $\beta = L_1/(L_1+L_2+L_g)$. Keeping the same filter inductances and considering an initial L_g = 0, β = 485/(485+125) = 0.8 is yielded from (6). For splitting, the filter capacitance is slightly adjusted to C = 10 μF, with $C_1 = (1-\beta)C$ = 2 μF and $C_2 = \beta C$ = 8 μF. This filter setting is identified as Filter II, as shown in Table II.

TABLE II
PARAMETERS OF THE PROTOTYPE

System Parameters			
Input voltage V_{in}	360 V	Fundamental frequency f_o	50 Hz
Grid voltage (RMS) V_g	220 V	Switching frequency f_{sw}	10 kHz
Output power P_o	6 kW	Sampling frequency f_s	20 kHz

***LCCL* Filter Parameters**				
Filter	Inverter-side inductor L_1	Filter capacitor C_1	Filter capacitor C_2	Grid-side inductor L_2
I (proposed)	485 μH	4.7 μF	4.7 μF	125 μH
II (conventional)	485 μH	2 μF	8 μF	125 μH

Recalling $T_{iL2}(z)$ in (9), the pole map of the closed-loop transfer function $T_{iL2}(z)/[1+T_{iL2}(z)]$ is drawn in Fig. 9, with L_g varying up to 2.6 mH (the pairs of closed-loop poles introduced by the PR regulator are not shown here since they vary little). As $T_{iL2}(z)$ is the loop gain related to i_{L2}, the closed-loop pole trajectory directly indicates the stability of grid current. With λ = 1, $f_{crit} = f_s/6$ and L_{g_crit} = 360 μH can be obtained from (12) and (15), respectively. For $\beta = \beta_{opt}$ = 0.5, as shown in Fig. 9(a), the resonant poles almost stay inside the unit circle, with only a critical point located exactly at the unit circle for $L_g = L_{g\_crit}$ = 360 μH ($f_r = f_s/6$). While for β = 0.8, as shown in Fig. 9(b), the resonant poles start exactly at the unit circle and then move outside for L_g < 850 μH. Thus, the grid current is not only critically stable at the initial status, but turns to be unstable for a wide range of grid impedance. This is consistent with the analysis in Section III, and confirms that the proposed method is more robust.

As mentioned in Section III, the critically stable point at L_g = 360 μH can be damped by the parasitic resistors in the filter and the grid. To illustrate this effect, the capacitor equivalent series resistor (ESR) R_C is taken as an instance, as shown in Fig. 10(a). With the increase of R_C, the resonant poles are shifted into the unit circle gradually. For the selected capacitor, R_C = 10 mΩ is given in [40]. Its corresponding pole locations are 0.49 ± j0.86, whose distance to the origin is 0.99. This stability margin seems small, but its robustness is not trivial. As β is the most important term on stability, the pole movement against the variation of β, which is caused by the capacitance deviation, is studied here, as shown in Fig. 10(b).

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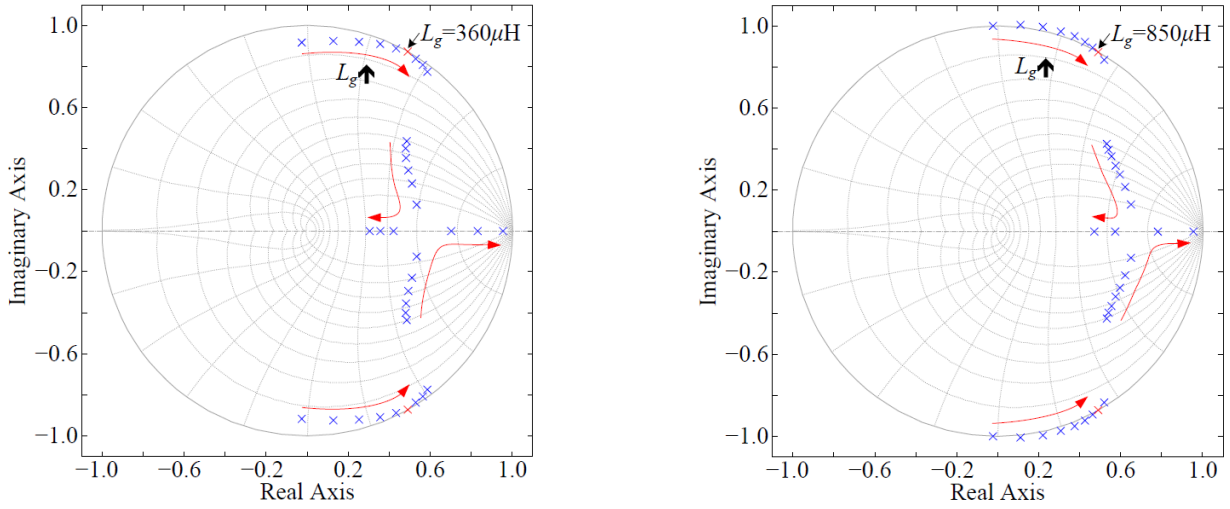
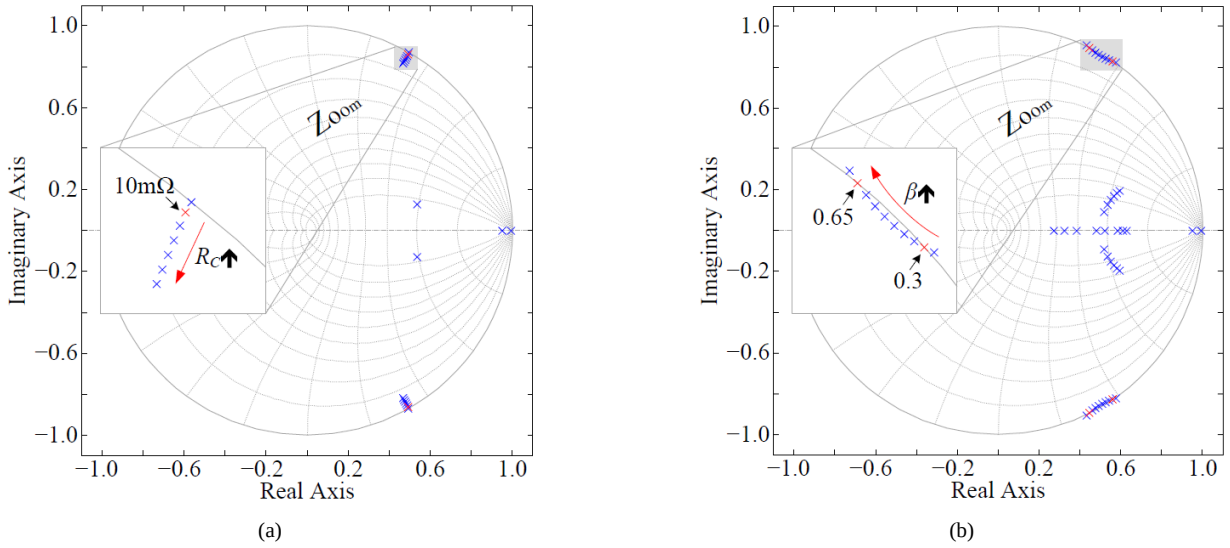


(a) (b)

Fig. 9. Grid current closed-loop pole maps with L_g varying up to 2.6 mH. (a) $\beta = L_1/(L_1+L_2+L_{g\_crit}) = 0.5$. (b) $\beta = L_1/(L_1+L_2+L_g) = 0.8$ (initialized with $L_g = 0$).



(a) (b)

Fig. 10. Damping of the critically stable point at $L_g = L_{g_crit} = 360\ \mu$H. (a) Effect of the capacitor ESR. (b). Effect of the capacitance deviation with $R_C = 10$ mΩ.

With $R_C = 10$ mΩ, the allowable range of β is 0.3 ~ 0.65, i.e., −40% ~ +30%, which is much wider than the possible range of the capacitance deviation (usually ±10% [40]), implying a good robustness. In practice, the robustness is even better due to other resistors in the filter inductors and the grid.

B. Experimental Results

Referring to the design procedure developed above, experimental results of the proposed and conventional weighted average current control schemes were compared here. The inverter current i_{L1}, the grid current i_{L2}, and their weighted average value i_{WA} were all measured. Transient performances of the two control schemes were tested at first. Usually, the transient response against load change was concerned for a power converter. However, for the grid-connected inverter which injected current into the grid, there was no physical "load", and its dynamics was evaluated by changing the current reference. Fig. 11 shows the experimental results when the current reference steps from half to full loads at $L_g = 0$. To achieve a detailed study, the experimental waveforms during the transition fundamental period are zoomed in, as shown in Figs. 11(b) and 11(d). It can be seen that satisfactory transient responses are performed in all the currents for $\beta = \beta_{opt} = 0.5$. With regard to i_{L2}, the percentage overshoot and the settle time are measured as 25% and 0.8 ms (5% tolerance), respectively, and the current ripple is 0.5 A, which is negligible. While for $\beta = 0.8$, quite different features are observed in i_{WA} and i_{L2} (i_{L1}). Despite that i_{WA} exhibits satisfactory steady-state and dynamic performances, i_{L1} and i_{L2} are both critically stable. When the current reference steps upward, both i_{L1} and i_{L2} oscillate, and the oscillations decay sluggishly and last for over two fundamental periods. The maximum current ripple in i_{L2}, which is identified by Δi_m in Fig. 11(d), is measured as 22 A (peak-to-peak).

Fig. 12 shows the experimental results at full load under the grid impedance variation. Both $L_g = 360\ \mu$H (the critical grid inductance) and $L_g = 2.6$ mH are tested here. For $\beta = \beta_{opt} = 0.5$, as shown in Fig. 12(a), stable operations are retained for both grid conditions, with a negligible current ripple of 0.5 A in i_{L2}. However, for $\beta = 0.8$, as shown in Fig. 12(b), disastrous

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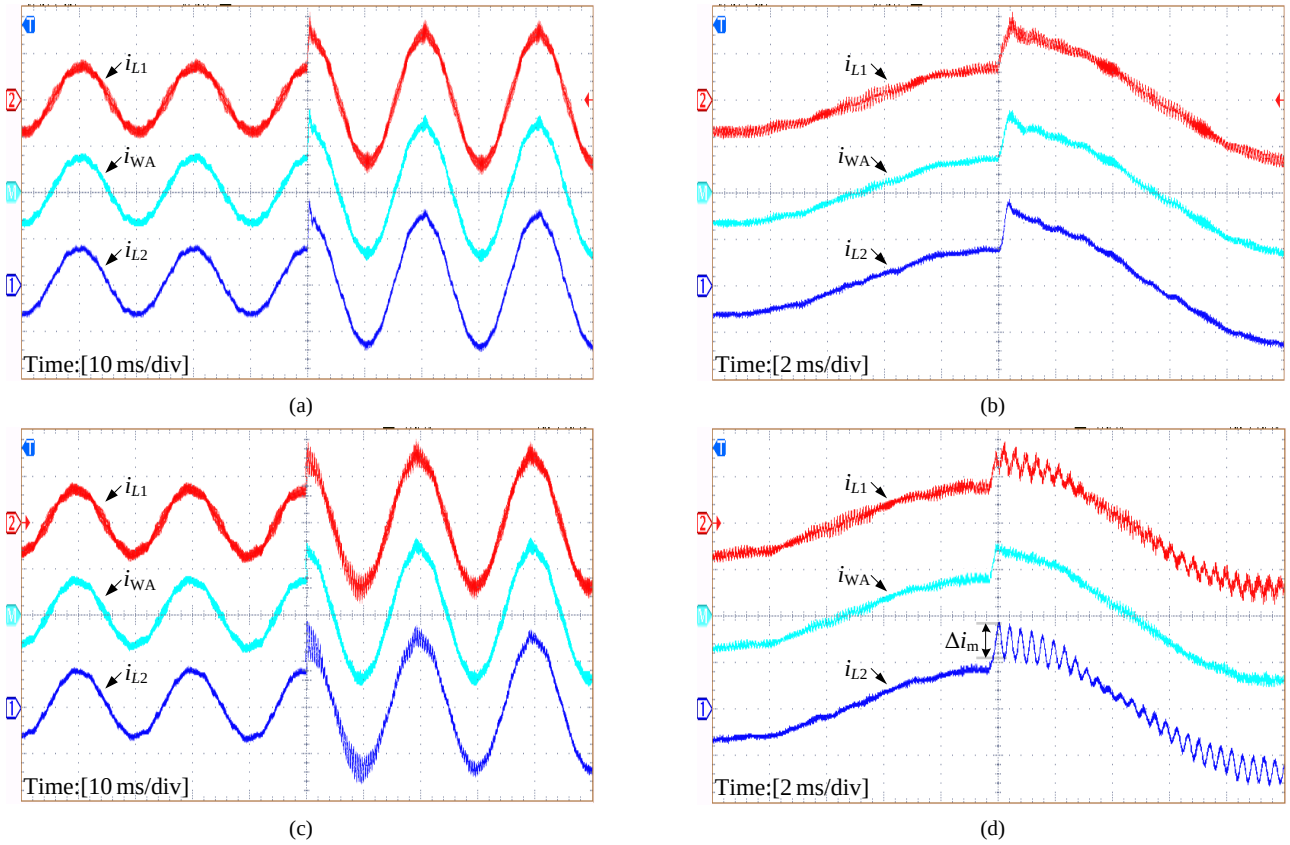

Fig. 11. Experimental results when the current reference steps from half to full loads at L_g = 0. (a) β = $L_1/(L_1+L_2+L_{g\_crit})$ = 0.5. (b) Zoom of (a). (c) β = $L_1/(L_1+L_2+L_g)$ = 0.8 (initialized with L_g = 0). (d) Zoom of (c). Current waveform scales: 30 A/div.

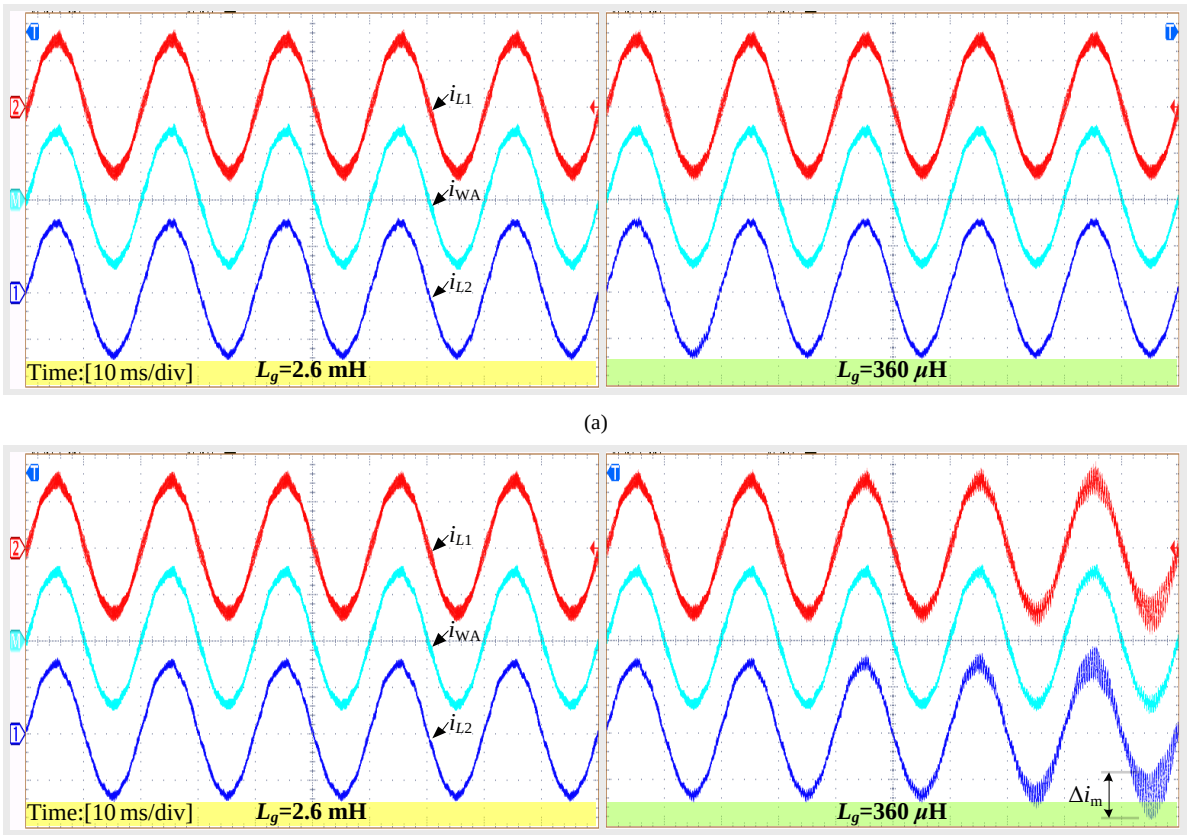

Fig. 12. Experimental results at full load under the grid impedance variation. (a) β = $L_1/(L_1+L_2+L_{g\_crit})$ = 0.5. (b) β = $L_1/(L_1+L_2+L_g)$ = 0.8 (initialized with L_g = 0). Current waveform scales: 30 A/div.

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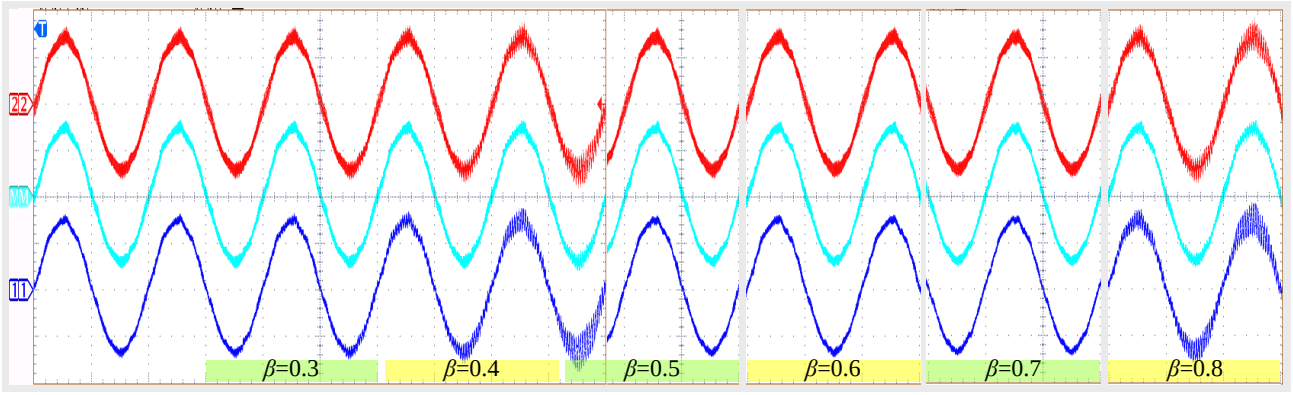
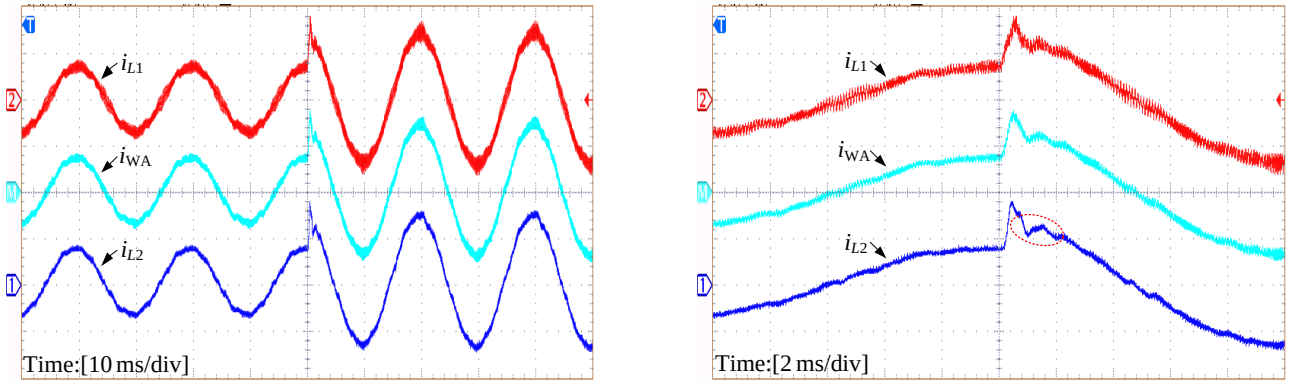


Fig. 13. Experimental results at L_g = 360 μH under the capacitance deviation. Current waveform scales: 30 A/div, time scale: 10 ms/div.



(a) (b)

Fig. 14. Experimental results when the current reference steps from half to full loads at L_g = 0 for λ = 0.5 and $\beta = \beta_{opt}$ = 0.5. (a) Full view. (b) Zoom of (a). Current waveform scales: 30 A/div.

oscillations are triggered when L_g = 360 μH, and the maximum current ripple in i_{L2} is measured as 30 A. It can be found that the proposed method achieves a strong robustness, which is in agreement with the theoretical analysis in this paper.

For L_g = 360 μH, system performances under the capacitance deviation was intentionally investigated here. In this test, the capacitances C_1 and C_2 were adjusted so that β was varied in the range from 0.2 to 0.8 with a step of 0.1. Fig. 13 shows the corresponding experimental results at full load. It can be seen that severe oscillations arise for β = 0.2 and β = 0.8, while stable operations are retained for all the other β. The practically allowable range of β is wider than that in Fig. 10(b), since there are extra resistors in the filter inductors and the grid except for the capacitor ESR.

The above results had verified the effectiveness of the proposed method under the dual-update mode, i.e., λ = 1. To show its generality, the single-update mode with λ = 0.5 was further tested. In this case, $f_s = f_{sw}$ = 10 kHz was set, and the *LCCL* filter designed in Section IV was adopted. Fig. 14 shows the experimental results when the current reference steps from half to full loads at L_g = 0. Stable operation is retained as expected. The percentage overshoot and the settle time in i_{L2} are measured as 25% and 2 ms, respectively. Compared with λ = 1, the dynamic response becomes slower, since the control bandwidth is reduced by the increased time delay. The other results under different grid conditions are similar to those in λ = 1, thus they are not repeated here. The experimental results confirm that the proposed method is effective irrespective of the time delay.

VI. Conclusion

This paper studies the robust single-loop current control scheme for the *LCL*-type grid-connected inverter. The weighted average current control implemented with the *LCCL* filter method is in focus, and it is proved to experience a poor robustness against the grid impedance variation and have weak stability (critically stable) in the grid current. To address these limitations, the single-loop weighted average current control is equivalently transformed into the dual-loop grid current control with an inherent capacitor current active damping. This inherent damping is determined by the capacitor split proportion. A design procedure is thus presented to select an optimal split proportion, so that a robust damping performance can be achieved by the inherent damping. Furthermore, with an improved *LCCL* filter configuration, the optimal split proportion is specified to 0.5. Thus, two equal nominal capacitances can be used for the split capacitors, which are very convenient for the practical implementation. Compared with the conventional single-loop control schemes, the proposed weighted average current control improves the system robustness without any extra cost, and it is applicable to the systems with different time delays. The effectiveness of the proposed method is verified by experimental results in a single-phase grid-connected inverter.

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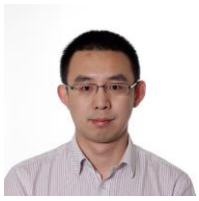

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